CLAIMS

What is claimed is:

1. A semiconductor integrated circuit for processing a plurality of received broadcast signals, the broadcast signals being of a type each having a different respective known digital code, the semiconductor integrated circuit comprising:

a digital sampler;

a memory arrangement; and

a plurality of correlators, being arranged to be operable in two modes wherein:

in an acquisition mode:

the digital sampler samples the received broadcast signals to produce a digital bit stream at a first bit rate;

the memory arrangement receives the digital bit stream and outputs at a second bit rate, being higher than the first bit rate;

the plurality of correlators receive the digital bit stream at the second bit rate, and each of the plurality of correlators correlates the reduced digital bit stream with a same locally generated version of one of the different known digital codes; and

in a tracking mode:

the digital sampler samples the received broadcast signals to produce a digital bit stream at the first bit rate and provides that digital bit stream direct to each of the plurality of correlators, each correlator correlates that digital bit stream with a different locally generated version of one of the known digital codes.

2. A semiconductor integrated circuit according to claim 1 wherein the memory arrangement comprises a circulating shift register.

3. A semiconductor integrated circuit according to claim 2 wherein the circulating shift register receives the digital bit stream at a rate equal to the first bit rate and circulates at the second bit rate.

4. A semiconductor integrated circuit according claim 1 wherein the memory arrangement comprises two shift registers arranged to alternately receive the digital bit stream while another of the shift registers circulates at the second bit rate.

5. A method of processing a plurality of received broadcast signals each showing a different respective digital code, the method comprising:

sampling the received broadcast signals to produce a digital bit stream at a first bit rate;

providing the digital bit stream at a second bit rate by reading into a memory arrangement at the first bit rate and reading out at the second bit rate;

correlating the digital bit steam at the second bit rate using a plurality of correlators each correlating the reduced digital bit stream with a same one of a locally generated version of the digital codes to acquire the broadcast signals; and

subsequently correlating the digital bit stream at the first bit rate using the plurality of correlators each correlating the reduced digital bit stream with a locally generated version of a different one of the digital codes to track previously acquired broadcast signals.

6. A method according to claim 5 wherein providing the digital bit stream at the second bit rate comprises circulating successive portions of the bit stream in a circulating shift register at the second bit rate.

7. A method according to claim 5 wherein providing the digital bit stream at the second bit rate comprises alternately reading the bit stream into one of

two shift registers while another of the two shift registers circulates at the second bit rate.

8. An apparatus to process a plurality of received broadcast signals having digital codes, the apparatus comprising:

a sampler to sample the received broadcast signals to produce a digital bit stream at a first bit rate in an acquisition mode;

a memory unit coupled to the sampler to receive the digital bit stream therefrom and to output the digital bit stream at a second bit rate in the acquisition mode; and

a correlator unit coupled to the memory unit to receive the digital bit stream at the second bit rate and to correlate the received digital bit stream with one of the digital codes in the acquisition mode, and wherein the sampler can directly provide the digital bit stream at the first bit rate to the correlator unit in a track mode to allow the correlator to correlate that bit stream to a different one of the digital codes.

9. The apparatus of claim 8 wherein the correlator unit comprises a plurality of correlators, each to correlate the received digital bit stream with a same one of the digital codes.

10. The apparatus of claim 8 wherein the one of the digital codes used in the correlation in the acquisition mode comprises a locally generated version of the digital code.

11. The apparatus of claim 8 wherein the one of the digital codes used in the correlation in the track mode comprises a locally generated version of the digital code.

12. The apparatus of claim 8 wherein the second bit rate is higher than the first bit rate.

13. The apparatus of claim 8 wherein the memory unit comprises a circulating shift register.

14. The apparatus of claim 13 wherein the circulating shift register is coupled to receive the digital bit stream at the first bit rate and to circulate at the second bit rate.

15. The apparatus of claim 8 wherein the memory unit comprises a plurality of shift registers to alternately receive the digital bit stream at the first bit rate, while another of these shift registers circulates at the second bit rate.

16. A system for processing a plurality of received broadcast signals having digital codes, the system comprising:

a means for sampling the received broadcast signals to produce a digital bit stream at a first bit rate;

a means for receiving the digital bit stream at the first bit rate and for producing the digital bit stream at a second bit rate;

a means for correlating the digital bit stream at the second bit rate with one of the digital codes to acquire the broadcast signals; and

a means for correlating the digital bit stream at the first bit rate with a different one of the digital codes to track the acquired broadcast signals.

17. The system of claim 16 wherein the means for producing the digital stream at the second bit rate comprises a means for circulating successive portions of the bit stream at the second bit rate.

18. The system of claim 16 wherein the means for producing the digital stream at the second bit rate comprises a means for alternately reading the bit stream into a plurality of shift registers while one of these shift registers circulates at the second bit rate.

19. The system of claim 16 wherein the means for correlating the bit streams at the first and second bit rates comprises a plurality of correlator means for respectively correlating the bit streams with locally generated versions of the digital codes.

20. The system of claim 16 wherein the second bit rate is higher than the first bit rate.